We claim:

1. A multimode clock recovery circuit for providing constant bit rate services in a cell relay network, comprising an embedded digital phase locked loop including an input circuit capable of generating a phase signal from at least two types of input signal, said phase signal controlling the output of said phase locked loop to generate clock signals for said constant bit rate services.

2. A multimode clock recovery circuit as claimed in claim 1, wherein said input circuit is adapted to receive a phaseword from a receive buffer for incoming cells to permit clock adaptive recovery based on the fill level of the receive buffer for incoming cells.

3. A multimode clock recovery circuit as claimed in claim 2, wherein said phaseword is derived from the write_pointer – read_pointer – *average*, where *average* is a parameter set by the user.

4. A multimode clock recovery circuit as claimed in claim 3, wherein the input circuit comprises a phase detector having a first input for receiving a feedback signal from the output of the phase locked loop and at least one additional input for receiving either a clock signal or a timestamp signal, said phase locked loop being adaptable to either type of said input signal.

5. A multimode clock recovery circuit as claimed in claim 4, wherein said phase detector comprises a common up/down counter.

6. A multimode clock recovery circuit as claimed in claim 5, wherein the common up/down counter does not wrap around and the output of the common up/down counter is fed to an accumulator to track the output of the up/down counter without applying a modulo function.

7. A multimode clock recovery circuit as claimed in claim 6, wherein the weighted output is fed to the accumulator.

8. A multimode clock recovery circuit as claimed in claim 6, wherein the weighted output of the up/down counter can be changed for receiving either a clock signal or a signal from a timestamp circuit.

9. A multimode clock recovery circuit as claimed in claim 8, wherein the weight of said up/down counter is programmable to sixteen for a timestamp signal and one for a clock signal.

10. A multimode clock recovery circuit as claimed in claim 8, further comprising first and second difference circuits, each receiving an SRTS input signal and an SRTS input signal delayed by one cell, the first circuit receiving its SRTS form the network, and the second difference circuit receiving its SRTS signal from a local SRTS generator, the first difference circuit providing an input to said up/down counter and the second difference circuit providing an input to a subtractor, the output of said difference circuit being fed to said accumulator with the weighted output of said up/down counter.

11. A multimode clock recovery circuit as claimed in claim 5, further comprising a local synchronous residual timestamp (SRTS) generator in the feedback loop of the phase locked loop.

12. A multimode clock recovery circuit as claimed in claim 11, wherein said local SRTS generator comprises a divider for receiving a feedback signal from the output of the phase locked loop, a counter for receiving the network clock signal, and a register for generating a local SRTS signal.

13. A multimode clock recovery circuit as claimed in claim 11, wherein the up/down inputs of the counter receive the respective network clock signal and the local SRTS signal.

14. A multimode clock recovery circuit as claimed in claim 1, wherein the phase locked loop goes into holdover mold wherein the output of the phase locked loop remains constant when a valid input signal is lost so as to maintain a constant frequency based on the last valid input signal.

15. A multimode clock recovery circuit as claimed in claim 1, wherein the phase locked loop goes into holdover mode when any of the following conditions occur: receive buffer runs out of SRTS values in the SRTS mode, a virtual circuit through said network times out, and loss of synchronization is asserted in a line rate mode.

16. The use of a multimode clock recovery circuit as claimed in claim 1 to filter an input clock prior to the generation of SRTS timestamps.

17. A multimode clock recovery circuit as claimed in claim 11, wherein the output of said clock recovery phase locked loop is fed to the input of said SRTS generator to de-jitter incoming clock signals.

18. A multimode clock recovery circuit for use in providing constant bit rate services in a cell relay network, comprising a phase detector having multiple inputs, a loop filter receiving the output of said phase detector, a digital controlled oscillator receiving the output of said loop filter, a jitter reduction circuit receiving the output of said digital controlled oscillator, a divider receiving the output of said jitter reduction circuit, and an SRTS generator in the feedback loop of said digital controlled oscillator.

19. A phase detector for recovering clock signals from received time stamps in a cell relay network providing constant bit rate services, comprising a first input for receiving a remote time stamp signal, a second input for receiving a locally generated time stamp signal, comparators for comparing the current time stamps with the previous time stamps to generate a carry signal, a weighted up/down counter receiving the inputs of said respective comparators, a subtractor for deriving the difference of said remote and locally generated time stamps, and an accumulator for adding the output of said subtractor to the output of said up/down counter to generate a phase output.

20. A phase detector as claimed in claim 18 having an error input for receiving an error flag to disable the counter when an error occurs.

21. A phase detector as claimed in claim 19, further comprising a register connected to the output of said adder for temporarily storing the phase output.

22. A method of recovering clock signals in a cell relay network providing constant bit rate services, comprising the steps of receiving incoming signals in a multimode phase locked loop (PLL), and placing said phase locked loop into holdover when the receive buffer runs out in SRTS mode, the virtual circuit times out in adaptive mode, and loss of sync is asserted in the line rate mode.

23. A method of recovering clock signals in a cell relay network wherein a phase signal is generated from an input signal and a locally generated signal in a phase locked loop, comprising the steps of detecting the phase difference between the input signal and a feedback signal by feeding said signals, or derivatives thereof, to a non-wrap around

up/down counter, and accumulating the absolute output of said up/down counter to create a phase output signal.

24. A method as claimed in claim 23, wherein the input to said up/down counter is switchable between a pair of difference circuits and a pair of sampling circuits to receive respectively SRTS and input clock signals.